The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union’s Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

This work is part of AIDA-2020 Work Package 7: Advanced hybrid pixel detectors.

The electronic version of this AIDA-2020 Publication is available via the AIDA-2020 web site <http://aida2020.web.cern.ch> or on the CERN Document Server at the following URL: <http://cds.cern.ch/search?p=AIDA-2020-D7.7>
**Abstract:**
Summary of the main results concerning the characterization of Active Edge Pixel Planar Sensor (AE-PPS) and pixel sensors with vertical etched electrodes (3D-PS). Most of the results here presented come from the testing of sensor from the AIDA-2020 common runs interconnected to the small-pixel-cell RD53A readout ASIC designed by the RD53 collaboration which is in charge of the development of the pixel front-end ASIC for the High-Luminosity upgrade of the LHC.

<table>
<thead>
<tr>
<th>Document identifier:</th>
<th>AIDA-2020-D7.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Due date of deliverable:</td>
<td>End of Month 52 (August 2019)</td>
</tr>
<tr>
<td>Justification for delay:</td>
<td>Delay on the mask layout of the planar run</td>
</tr>
<tr>
<td>Report release date:</td>
<td>31/12/2019</td>
</tr>
<tr>
<td>Work package:</td>
<td>WP7: Advanced hybrid pixel detectors</td>
</tr>
<tr>
<td>Lead beneficiary:</td>
<td>MPP-MPG</td>
</tr>
<tr>
<td>Document status:</td>
<td>Final</td>
</tr>
</tbody>
</table>

**Final Pixel Characterization**

**Deliverable: D7.7**
AIDA-2020 Consortium, 2019
For more information on AIDA-2020, its partners and contributors please see www.cern.ch/AIDA2020

The Advanced European Infrastructures for Detectors at Accelerators (AIDA-2020) project has received funding from the European Union’s Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168. AIDA-2020 began in May 2015 and will run for 4 years.

### Delivery Slip

<table>
<thead>
<tr>
<th>Name</th>
<th>Partner</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Authored by</td>
<td>A. Macchiolo</td>
<td>12/10/19</td>
</tr>
<tr>
<td></td>
<td>I. Vila</td>
<td></td>
</tr>
<tr>
<td>Edited by</td>
<td>I. Vila</td>
<td>12/10/19</td>
</tr>
<tr>
<td>Reviewed by</td>
<td>D. Bortoletto</td>
<td>18/12/19</td>
</tr>
<tr>
<td>Approved by</td>
<td>Scientific coordinator</td>
<td>31/12/19</td>
</tr>
<tr>
<td></td>
<td>Steering Committee</td>
<td></td>
</tr>
</tbody>
</table>
# TABLE OF CONTENTS

EXECUTIVE SUMMARY .............................................................................................................. 4

1. RESULTS OBTAINED WITH FBK 3D SENSORS .................................................................... 4

2. RESULT OBTAINED WITH 3D SENSORS OF IMB-CNMs .................................................... 6

3. RESULTS OBTAINED WITH ACTIVE EDGE PLANAR SENSORS ........................................ 7
EXECUTIVE SUMMARY

Summary of the main results concerning the characterization of Active Edge Pixel Planar Sensor (AE-PPS) and pixel sensors with vertical etched electrodes (3D-PS) are reported here. Most of the results presented come from the testing of sensor from the AIDA-2020 common runs interconnected to the small-pixel-cell RD53A readout ASIC designed by the RD53 collaboration which is in charge of the development of the pixel front-end ASIC for the High-Luminosity upgrade of the LHC.

Key results summarized here are:
- Excellent radiation tolerance of small-pixel-cell 3D-PS up to hadron fluences suitable for the HL-LHC vertex detectors.
- Boosted hit efficiency of several AE-PPS technological incarnations for tracks hitting the sensor very close to its physical edge.

1. RESULTS OBTAINED WITH FBK 3D SENSORS

Beam tests analysis have been performed with the FBK 3D sensors of the AIDA-2020 common run. The production of 3D pixel sensors at FBK has been carried out on SOI and Si-Si Direct Wafer Bonding (DWB) wafers of 6-inch diameter with an active thickness of 130 μm and a handle wafer thickness of 500 μm. The 3D process is single sided. The layout of the wafer is shown in figure 1.

![Figure 1: Wafer layout of 3D pixel sensor from the FBK AIDA-2020 common run.](image)

The focus of these studies has been on RD53A sensors, with 50×50 or 25×100 μm² pitch, the latter being available in two versions with 1 (1E) or 2 (2E) read-out columns. These are the two pixel-cell form factors that are being considered for the new pixel systems of the ATLAS and CMS experiment at HL-LHC. This study was performed with the RD53A ASIC.

While the 50×50 μm² and the 25×100 μm² (1E) designs are relatively easy with the considered technology, the 25×100 μm² (2E) design is quite challenging due to the bump-bonding pad, whose...
size cannot be significantly reduced. The situation is further complicated due to the bump pad configuration in the RD53A chip, which follows a 50×50 µm² regular pattern.

The sensors were interconnected to the RD53A chip by flip-chipping at Fraunhofer IZM (Germany). The modules have been irradiated at CERN-PS with a 24 GeV proton beam, which has a FWHM of 12 mm in the x- and y-directions, at a nominal fluence of $10^{16}$ n$_{eq}$/cm$^2$.

Even if the modules were tilted in the beam at an angle of 55° to irradiate the ~2x1 cm$^2$ sensor area the irradiation was not homogeneous. The target fluence was only reached in a limited central area where the sensor columns are interconnected to the Linear Front-End section of the RD53A chip (see Figure 2). The beam test was carried out at CERN-SPS with 60 and 120 GeV protons. Track reconstruction was performed using the AIDA telescope software framework. Figure 1 shows the different fluence regions that were analysed on a module with 25x100 µm$^2$ pixel cells.

In the following, the results of the hit efficiency will be quoted for only the Linear FE section of the RD53A chip. The hit efficiency for the irradiated module, with a pixel cell of 25x100 µm$^2$, at a bias voltage of 125V, is shown in Figure 3, at three different fluence levels. The results are relative to a perpendicular incidence of the beam. Irradiated 3D-PS sensors were operated at a bias voltage of 125 V and a temperature of -36 C.

The hit efficiency for a module with a 50x50 µm$^2$ pixel cell, is shown in Figure 4. As in the case of the 25x100 µm$^2$ pixel cell, the efficiency remains very high and is almost unaffected by the fluence. The bias voltage was 141 V at a temperature of -36 C for the irradiated sensors, the non-irradiated

Figure 2: Fluence map for a 3D module with a pixel pitch of 25x100 µm$^2$ in the area of the module interconnected to the linear section of the RD53A read-out chip

Figure 4: Hit efficiency for a module with a pixel cell of 50x50 µm$^2$
sensor has a bias voltage of 15 V. The areas of lower efficiency are due to the presence of the etched columnar electrodes, the full efficiency was recovered by tilting the sensor by a few degrees.

Figure 3: Cell map of the hit efficiency for a module of 25x100 $\mu m^2$ pitch, in the three fluence regions defined in Figure 2.

Figure 4: Cell map of the hit efficiency at normal incidence for a module of 50x50$\mu m^2$ pitch, at fluence levels of $\sim 4 \times 10^{15}$ $n_{eq}/cm^2$, $8.5 \times 10^{15}n_{eq/cm^2}$ and $10^{16}n_{eq/cm^2}$. The hit efficiency observed is quoted on top of the maps.

2. RESULT OBTAINED WITH 3D SENSORS OF IMB-CN M

In February 2019, a second AIDA-2020 3D-PS common run was completed at the IMB-CN M premises. Seven Si-on-Si wafers (10 cm in diameter) were processed with an active (high-resistivity
bulk) thickness of 150 μm from a total physical thickness of 350 μm. The 3D-PS sensors were manufactured using a single-sided n-in-p technology. The sensor layout was compatible with the RD53A readout ASIC. Three different pixel cell designs were manufactured: square pixel cells (50x50 μm²) with one single junction column (3D-PS) and rectangular pixel cells (25x100 μm²) with either one single columnar junction (1E) or two columnar junctions (2E).

The manufacturing yield of the square 3D-PS sensors was of 79% (50 out of 63). The yield for the 1E and 2E sensors was of 50% (7 out of 14) and 6% (4 of 63) respectively. The yield was based on the electrical characterization (IV and CV) on wafer of each sensor before dicing. The electrical characterization was carried out on diodes and on RD53A compatible sensors using a temporary metal layer to bias them, the metal layer was removed after the testing (see Figure 5). On the selected sensors, the reverse current per pixel was below 25 pA.

The limited availability of the RD53A ASIC delayed the interconnection of the sensors to the electronics until September 2019. A total of 26 single sensors interconnected to RD53A ASIC are currently available to be measured in beam tests at DESY and FERMILAB starting in November 2019. Moreover, five pseudo-double sensors, i.e. two adjacent single sensors diced together, will be mounted in the first prototypes of the High-Density Interconnects to carry out dedicated serial powering studies.

![Figure 5](image1.png)

*Figure 5 CV and IV characterization of diodes included in the IMB-CNMB 3D manufacturing run to assess the quality of the production.*

### 3. RESULTS OBTAINED WITH ACTIVE EDGE PLANAR SENSORS

Given the delays in the production of the WP7 common run of planar sensors with active edges, we report the results obtained with the previous prototyping run at FBK. This production differs from the common WP7 run in the shape of the trenches. While in the final production these will have a continuous shape, in the first run the trenches are implemented with a staggered geometry (see Figure 6), as a sequence of 5 μm wide and 40 μm long individual units. This feature results in a less challenging post-processing of the wafers, during the etching of the mechanical wafer. The staggered trenches avoid the spontaneous separation of the devices from the main silicon slab when the back-thinning reaches the bottom of the trench at the wafer to wafer interface. As a drawback this design needs the implementation of a dicing line external to the trench position, leading to a wider inactive region at the periphery of the sensor.
This production has been carried out at FBK on SOI and SiSi Direct Wafer Bonding (DWB) wafers of 6-inch diameter with an active thickness of 100 and 130 µm.

![Image](image.jpg)

*Figure 6: Image of the staggered structure of the trench, at a 50 µm distance from the last pixel. The sensor active thickness is 130 µm.*

After interconnection of the sensor to the ATLAS FE-I4 read-out chip, test beam studies have been performed at DESY with 4 GeV electrons before and after an irradiation to a fluence of $3 \times 10^{15}$ n$_{eq}$/cm$^2$. The most important requirement for active edge pixel detectors is to show that pixel efficiency remains high in the region close to the sensor edge. The projected hit efficiency in the region of the trench for a module before irradiation is shown in Figure 7. The hit efficiency follows the structure of the staggered trenches and its value is still above 50% up to 44 µm from the last pixel. After irradiation at $3 \times 10^{15}$ n$_{eq}$/cm$^2$ with 23 MeV protons, the hit efficiency above the pixel implant, at a bias voltage of 100V, decreases from 99% to 97% (Figure 7b). The edge of the last column of pixels correspond to the point at 20000 µm on the horizontal axis of the plots, showing the distance from the first column of pixels; the trenches are further displaced to the right, at about 20050 µm. The plot shows that the hit efficiency is still significant even in the region between the last pixel column and the trench.

Sensors of the same production, with a geometry compatible with the RD53A chip, but without active edges, have been tested at the beam test in DESY. Two modules, with and without Punch-Through (PT) structure, both with a sensor thickness of 100 µm and a pixel cell of 50x50 µm$^2$, have been compared after irradiation with 23 MeV protons at a fluence of $5 \times 10^{15}$ n$_{eq}$/cm$^2$. The module without PT achieves a higher hit efficiency of 99.5% at perpendicular incidence at a bias voltage of 300V. The module with PT yields a lower efficiency of 97.5%, up to a higher bias voltage of 400V. The loss of efficiency, due to the PT structure, can be recovered when tilting the detector with respect to the beam, reaching a value of 99% already at an angle of 15° (see Figure 8).
Figure 7: (a) 2-D projection of the hit efficiency close to trench region for a FE-I4 module before irradiation. The hit efficiency follows the structure of the trenches (represented as white rectangles). (b) Hit efficiency projected over the last pixel cell length and the trench region for a FE-I4 module with staggered trenches irradiated at a fluence of $3 \times 10^{15}$ $n_{eq}/cm^2$.

Figure 8 (a) Hit efficiency of two planar pixel modules, both with an active thickness of 100 µm and a pixel cell of 50x50 µm², one with and one without PT structure. The modules have been irradiated at a fluence of $5 \times 10^{15}$ $n_{eq}/cm^2$ at KIT. (a) Hit efficiency at perpendicular incidence as a function of the applied bias voltage (b) Hit efficiency of the module with PT as a function of the beam incidence angle at a bias voltage of 300V.